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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/560,706	07/24/2006	Takefumi Nishimuta	5000-5291	9357

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EXAMINER	
BELOUSOV, ALEXANDER	
ART UNIT	**PAPER NUMBER**
2811	

NOTIFICATION DATE	DELIVERY MODE
07/01/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/560,706	NISHIMUTA ET AL.	
	Examiner	Art Unit	
	ALEXANDER BELOUSOV	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,6 and 9-19* is/are pending in the application.

4a) Of the above claim(s) *14-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6 and 9-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed on 03/17/2008. Currently, claims 1-3, 5, 6 & 9-13 are pending.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim(s) 1-3, 5, 6 & 9-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claim limitations of "a semiconductor substrate comprising a projecting part of which surfaces are at least two different crystal planes on a principal plane", as recited in claim(s) 1, are unclear as to which element is formed on a principal plane.

The claim limitations of "a gate electrode **comprised** on said at least a part of each of said at least two different crystal planes constituting the surface of the projecting part so as to be electrically insulated therefrom by the gate insulator", as recited in claim(s) 1, are unclear as to what is the gate electrode comprised **of**.

The claim limitations of "a pair of diffusion regions having the same conductivity type and formed on **both sides** of the gate electrode", as recited in claim(s) 1, are unclear as to how the gate electrode can have only two sides. Alternatively, the claim limitations "both sides" lack antecedent basis.

The claim limitations of "a semiconductor substrate comprising a projecting part of which surfaces have at least two different crystal planes on a principal plane", as recited in claim(s) 5, are unclear as to which element is formed on a principal plane.

The claim limitations of "a semiconductor substrate comprising a projecting part of which **surfaces** ***have*** at least ***two different crystal planes*** on a principal plane; a gate insulator covering each of ***said two different crystal planes*** of the **surface** of said projecting part", as recited in claim(s) 5, are unclear as to whether multiple surfaces have two different crystal planes, or just a single surface.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claim(s) 1-3, 5, 6 & 9-13** are rejected under 35 U.S.C. 102(b) as being anticipated by (US-2003/0102497) by Fried et al ("Fried").

Regarding claim 1, Fried discloses in FIG. 7a-b and related text a MIS transistor (paragraph 2), comprising:

a semiconductor substrate (206) comprising a projecting part of which surfaces are at least two different crystal planes on a principal plane (Abstract and FIG. 7b; first surface, is the surface of 206 contacting 208; second surface, is the surface of 206 contacting 208; principal plane is the bottom surface of 206);

a gate insulator (208 & 210) for covering at least a part of each of said at least two different crystal planes constituting the surface of the projecting part;

a gate electrode (212) comprised on said at least a part of each of said at least two different crystal planes constituting the surface of the projecting part so as to be electrically insulated therefrom by the gate insulator; and

a pair of diffusion regions (paragraph 57; "the S/D **regions**… comprising the fin bodies") having the same conductivity type (inherent feature of S/D regions) and formed on both sides of the gate electrode (inherent feature of S/D regions) in the projecting part (paragraph 57; "the S/D regions… **comprising the fin bodies**") so as to face said at least a part of each of said at least two different crystal planes constituting the surface of the projecting part.

Regarding claim 2, Fried discloses in FIG. 7a-b and related text the channel width of a channel formed along with the gate insulator between the pair of diffusion regions is indicated by summation of each width of each channel formed along each of said at least two different crystal planes (see FIG. 7b).

Regarding claim 3, Fried discloses in FIG. 7a-b and related text the gate insulator covers said at least a part of each of said at least two different crystal planes, which configure the surface of the projecting part, so as to continuously cover said at least two different crystal planes (inherent: if the gate insulator did not continuously cover the surface of the projecting part, the gate electrode would short to the projecting part, and the device would not be operational).

Regarding claim 5, Fried discloses in FIG. 7a-b and related text the MIS transistor (paragraph 2) comprising:

a semiconductor substrate (206) comprising a projecting part of which surfaces have at least two different crystal planes on a principal plane (Abstract and FIG. 7b; first surface, is the surface of 206 contacting 208; second surface, is the surface of 206 contacting 208; principal plane is the bottom surface of 206);

a gate insulator (208 & 210) covering each of said two different crystal planes of the surface of said projecting part, said gate insulator further covering at least a part of said principal plane of said substrate (208 is above the bottom surface of 206; hence, "covering… principal plane");

a gate electrode (212) formed on said gate insulator so as to be electrically insulated from the semiconductor substrate; and

a pair of diffusion regions (paragraph 57; "the S/D **regions**… comprising the fin bodies") of the same conductivity type (inherent feature of S/D regions) formed at said two different crystal planes of said projecting part (paragraph 57; "**exposed** portions of the fins may be doped to form S/D regions"; the two different crystal planes **are** exposed from 208; see FIG. 7a-b) and at said principal plane of said substrate (the principal plane is also exposed from 208) on both sides of said gate electrode.

Regarding claim 6, Fried discloses in FIG. 7a-b and related text the gate insulator covers at least each of said at least two different crystal planes and the principal plane so that the principal plane and said two different crystal planes are continuously covered (inherent: if the gate insulator (208 & 210) did not continuously cover the semiconductor, the gate electrode would short to the semiconductor, and the device would not be operational; 208 is above the bottom surface of 206; hence, "covers… principal plane").

Regarding claims 9 & 10, Fried discloses in FIG. 7a-b and related text being a signal transistor (inherent: transistors can be "on" or "off", hence at least two different signals).

Regarding claims 11 & 12, Fried discloses in FIG. 7a-b and related text the semiconductor substrate is a silicon substrate (paragraph 44: "**any** semiconductor material") and the hydrogen content at an interface of the silicon substrate and the gate insulator is 10.sup.11/cm.sup.2 or less in units of surface density (Fried does not disclose **any** usage of hydrogen, hence the hydrogen content is "zero").

Regarding the process limitations recited in claims 11 & 12 ("the gate insulator **is formed by** exposing the surface of the silicon substrate to a plasma of a prescribed inert gas so as to remove hydrogen"), these would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claim 13, Fried discloses in FIG. 7a-b and related text the semiconductor substrate is a silicon substrate (paragraph 44: "**any** semiconductor material"), and

the principal plane and said at least two different crystal planes are any two different crystal planes from the (100) plane, the (110) plane and the (111) plane (paragraph 40).

Response to Arguments

Applicant's arguments filed on 03/17/2008 have been fully considered but they are not persuasive.

1. **Regarding claims 1 & 5**, the Applicant argues that the claims are not anticipated by Fried, because Fried does not disclose "a gate insulator for covering at least a part of **each** of said at least two different crystal planes constituting the surface of the projecting part".

Fried does anticipate claims 1 & 5 (see rejection above). Specifically, the elements 208 **& 210** of Fried **are** the gate insulator and the elements cover "at least a part of **each** of said at least two different crystal planes".

2. **Regarding claims 1 & 5**, the Applicant argues that the claims are not anticipated by Fried, because Fried does not disclose "semiconductor substrate **comprising** a projecting part".

Fried does anticipate claims 1 & 5 (see rejection above). Specifically, the elements 206 of Fried **are** parts of the SOI substrate, which is comprise of multiple projecting parts (see FIG. 7b).

Conclusion

1. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Belousov whose telephone number is 571-270-3209. The examiner can normally be reached on Monday - Thursday 7:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Alexander Belousov/
Examiner, Art Unit 2811

06/20/2008

/Ori Nadav/
Primary Examiner, Art Unit 2811